REMARKS/ARGUMENTS

Claims 1-25 were pending in this application when last examined by the Examiner. Claims 1-3, 5, 7-9, 16, 18, 20, and 22-23 have been amended. Claim 25 has been canceled. Claims 26-29 have been added. The amendments find full support in the original specification, claims, and drawings. No new matter has been added. In view of the above amendments and remarks that follow, reconsideration and an early indication of allowance of the now pending claims 1-24 and 26-29 are respectfully requested.

As an initial matter, Applicant encloses herewith a Decision Granting Petition dated June 11, 2007. The Decision grants Applicant's petition to correct the filing date from January 29, 2004, to January 20, 2004. Accordingly, Applicant respectfully requests that the USPTO records be updated to reflect the correct filing date.

Claim 16 is objected to because it recites a "bus" instead of a "PCI bus." Applicant has amended this claim to now recite a "PCI bus." Withdrawal of the objection is respectfully requested.

Claims 1, 2, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated or, in the alternative, under 35 U.S.C. 103(a) as obvious over "RIFLE-62: A Flexible Environment for Prototyping Dynamically Reconfigurable Systems," by Vasilko. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vasilko. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasilko in view of U.S. Patent No. 6,356,823 (Iannotti). Claims 9-19 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasilko in view of U.S. Patent No. 5,864,712 (Carmichael). Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vasilko in view of U.S. Patent No. 5,908,455 (Parvahan). Applicant respectfully traverses these rejections.

In continuing to reject the claims, the Examiner equates Vasilko's RIFLE-62 experimental board as the claimed "core board." In doing so, the Examiner contends that the claimed "second communication block" is the XC6200 external interface shown in figure 2 of Vasilko. (See, Office action, p. 3, 2nd par.). However, the Examiner does not state how

Vasilko's experimental board includes all of the other components required for the recited "core board," specifically, the claimed "one or more devices which simulate, by software, peripheral devices of the build-in microcomputer," and the claimed "computing block." Assuming, *arguendo*, that the FPGAs (XC6200, XC3000, or XC4013E) on the experimental board are the claimed "one or more devices," there is no "computing block" in the RIFLE-62 experimental board. (See, Vasilko, Figure 1).

The Examiner refers to the sections in Vasilko entitled "software environment," and "prototyping design flow" to contend that somewhere in this disclosure there is a teaching of the missing "computing block." However, the software environment discussed in Vasilko simply refers to code that is used to "facilitate low-level operations on the FIGLE-62 experimental board." (Section 5, 1st par.). The prototyping design flow refers to the prototyping of different applications that may be targeted for the RIFLE-62 platform. Such prototyping may use hardware or software design routes. However, nothing in this disclosure teaches or suggests that the RIFLE-62 platform is modified to include the claimed "computing block."

In order to further differentiate between the claimed invention and the disclosure in Vaskilko, claim 1 has been amended to recite "an interface board that includes a port assignment conversion board, a plurality of standard circuits, and a plurality of facility boards which are associated with hardware of said electronic control unit, said standard circuits and facility boards being selectable by said port assignment conversion board, and said port assignment conversion board being coupled to said core board via a harness." Support for this limitation is found in Applicant's specification on paragraph 0082 and in FIG. 5

Vasilko fails to teach or suggest the claimed "interface board." Vasilko's disclosure in section 3.2 of the interconnections between the FPGAs at most teaches a primary bus section and a second bus section connected via fast transceivers. However, Vasilko's busses and transceivers are not the claimed "port assignment conversion board, a plurality of standard circuits, and a plurality of facility boards." Accordingly, claim 1 is now in condition for allowance.

Independent claims 2, 22, and 23 include limitations that are similar to the limitations of claim 1 which make claim 1 allowable. Accordingly, claims 2, 22, and 23 are also in condition for allowance.

Claims 3-21 and 24 are in condition for allowance because they depend on an allowable base claim, and for the additional limitations that they contain.

Claims 26-29 are new in this application. Claims 26-29 are in condition for allowance because they depend on an allowable base claim, and for the additional limitations that they contain. Specifically, claim 26 recites that "the motherboard includes a first central processing unit, and the core board includes a second central processing unit." Support for this limitation is found in FIG. 4 of Applicant's disclosure. Vasilko fails to teach or suggest this limitation. As discussed above with respect to claim 1, no CPU is included in the RIFLE-62 experimental board. In fact, Vasilko teaches away from a system that would include such a CPU. Vasilko states that "[r]ather than integrating one specific processor on the RIFLE-62 board we opted to provide fast and flexible connection to all necessary on-board signals." (Section 3.5, par. 3). Thus, instead of integrating a specific processor, the RIFLE-62 board includes a microprocessor interface that allows access to an "embedded microprocessor system located on a daughter board." (Id.) (Emphasis added). Accordingly, claim 26 is also in condition for allowance for its added limitations.

Claim 27 adds the limitation that "each of the plurality of facility boards include a microcomputer for transferring data to and from the one or more devices." Support for claim 27 is found in Applicant's specification on paragraph 0083 and in FIG. 7 (reference 67). There is nothing in Vasilko's interconnections of the FPGAs to teach or suggested the claimed "microcomputer." Accordingly, claim 27 is also in condition for allowance for its added limitations.

Claim 28 adds the limitation that "the transferring of data to and from the one or more devices is based on a direct memory access technique." Support for claim 28 is found in Applicant's specification on paragraph 0083. Vasilko fails to teach or suggest this limitation. Accordingly, claim 28 is also in condition for allowance for this added limitation.

Claim 29 includes the limitation that "each of the plurality of facility boards include a microcomputer, and the method further comprises: transferring data to and from the one or more devices via the microcomputer." As discussed with respect to claim 27, Vasilko fails to teach or suggest this limitation. Accordingly, claim 29 is also in condition for allowance for this added limitation.

In view of the above amendments and remarks, reconsideration and an early indication of allowance of the now-pending claims 1-24 and 26-29 are respectfully requested.

Respectfully submitted,
CHRISTIE, PARKER & HALE, LLP

By _____
Josephine E. Chang
Reg. No. 46,083
626/795-9900

JEC/lal

Encl. Decision Granting Petition